

## NTE6402 Programmable Unijunction Transistor (PUT)

### **Description:**

The NTE6402 is a 3-terminal silicon planer passivated PNP device available in the standard plastic low cost TO98 and TO92 type packages. The terminals are designated as anode, anode gate, and cathode.

This device has been characterized as a Programmable Unijunction Transistor (PUT), offering many advantages over conventional unijunction transistors. The designer can select  $R_1$  and  $R_2$  to program unijunction characteristics such as intrinsic standoff ratio, Interbase resistance, peak-point emitter current, and valley-point current to meet his particular needs.

PUT's are specifically characterized for long interval timers and other applications requiring low leakage and low peak point current. PUT's similar types have been characterized

### **Applications:**

- SCR Trigger
- Pulse and Timing Circuits
- Oscillators
- Sensing Circuits
- Sweep Circuits

### **Absolute Maximum Ratings:** ( $T_A = +25^\circ\text{C}$ unless otherwise specified)

Gate-Cathode Forward Voltage .....	+40V
Gate-Cathode Reverse Voltage .....	-5V
Gate-Anode Reverse Voltage .....	+40V
Anode-Cathode Voltage .....	$\pm 40\text{V}$
DC Anode Current (Note 1) .....	150mA
Peak Anode, Recurrent Forward Current	
Pulse Width = 100 $\mu\text{s}$ , Duty Cycle = 1% .....	1A
Pulse Width = 20 $\mu\text{s}$ , Duty Cycle = 1% .....	2A
Peak Anode, Non-Recurrent Forward Current (10 $\mu\text{s}$ ) .....	$\pm 20\text{mA}$
Capacitive Discharge Energy (Note 2) .....	250 $\mu\text{J}$
Total Average Power (Note 1) .....	300mW
Operating Ambient Temperature Range (Note 1) .....	-50° to +100°C

Note 1. Derate currents and powers 1%/°C above 25°C.

Note 2.  $E = 1/2 CV^2$  capacitor discharge energy with no current limiting.

**Electrical Characteristics:** ( $T_A = +25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Peak Current	$I_P$	$V_S = 10\text{V}, R_G = 1\text{M}\Omega$	–	–	2	$\mu\text{A}$
		$V_S = 10\text{V}, R_G = 10\text{k}\Omega$	–	–	5	$\mu\text{A}$
Offset Voltage	$V_T$	$V_S = 10\text{V}, R_G = 1\text{M}\Omega$	0.2	–	1.6	V
		$V_S = 10\text{V}, R_G = 10\text{k}\Omega$	0.2	–	0.6	V
Valley Current	$I_V$	$V_S = 10\text{V}, R_G = 1\text{M}\Omega$	–	–	50	$\mu\text{A}$
		$V_S = 10\text{V}, R_G = 10\text{k}\Omega$	70	–	–	$\mu\text{A}$
		$V_S = 10\text{V}, R_G = 200\Omega$	1.5	–	–	mA
Anode Gate–Anode Leakage Current	$I_{GAO}$	$V_S = 40\text{V}, T_A = +25^\circ\text{C}$	–	–	10	nA
		$V_S = 40\text{V}, T_A = +75^\circ\text{C}$	–	–	100	nA
Gate–Cathode Leakage Current	$I_{GKS}$	$V_S = 40\text{V}, \text{Anode–Cathode Short}$	–	–	100	nA
Forward Voltage	$V_F$	$I_F = 50\text{mA}$	–	–	1.5	V
Pulse Output Voltage	$V_O$		6	–	–	V
Pulse Voltage Rate of Rise	$t_r$		–	–	80	ns

